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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,126	11/27/2001	Robert Conrad Malkemes	SAR 13895A	1964

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EXAMINER	
LUGO, DAVID B	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,126	MALKEMES ET AL.	
	Examiner	Art Unit	
	David B. Lugo	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/1/05 have been fully considered but they are not persuasive.

With respect to the rejection of claims 1, 4 and 9 under 35 U.S.C. 103(a), Applicant argues that Tsujimoto in combination with Win do not disclose spatially equalizing received spatially diverse replicas of the RF signal, temporally equalizing the combined spatially equalized signals, and adapting the equalized signal to the symbol error signal. The Examiner respectfully disagrees. The transversal filters 101 and 102 are configured to equalize the received first and second diversity signals. This constitutes spatially equalizing spatially diverse replicas of the RF signals. Further, the spatially equalized signals are combined via combiner 158, and are temporally equalized via decision feedback equalizer 105, and the spatial and temporal equalization is adapted via tap control circuits 103, 104 and 106 according to the error signal output from subtractor 109. Tsujimoto in combination with Win are thus considered to teach the limitations of claims 1, 4 and 9. Accordingly, the rejection is maintained.

With respect to claims 2-3, 5-8 and 10-13, Applicant argues that these claims are allowable because they possess the same claimed features of the claims from which they depend. Accordingly, since claims 1, 4 and 9 stand rejected, claims 2-3, 5-8 and 10-13 also stand rejected. The rejection of claims 1-13 is maintained, as indicated below.

With respect to the provisional double patenting rejections, the rejection will be maintained until a terminal disclaimer is filed.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 9/22/05 is being considered by the examiner. Two references in the "Other Documents" section have been crossed off as they were already cited in the IDS filed 3/14/02.

Claim Objections

3. Claims 7 and 11 are objected to because of the following informalities:

a. Claim 7, line 6, "MSLE" should be --MLSE--.

b. Claim 11, line 6, "MSLE" should be --MLSE--.

Appropriate correction is required.

Double Patenting

4. Claims 1 and 3 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of copending Application No. 09/776,078 in view of Win et al. U.S. Patent 6,804,312.

Regarding claims 1 and 3 of the instant application, claim 7 of the '078 application discloses the steps of receiving a plurality of spatially diverse replicas of an RF signal, and adaptively combining the spatially diverse replicas to generate an equalized signal.

Claim 7 of the '078 application does not expressly disclose that the receiver may be implemented in a computer readable storage medium containing a program.

However, it is well known in the art to implement a digital receiver using a program contained in computer readable storage medium. For instance, Win et al. disclose that a digital receiver for spatial processing that may be implemented with various software techniques (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the receiver using a software implementation where a computer program is stored in computer readable storage medium as a matter of design choice, as software and hardware implementations are well-recognized art equivalents.

This is a provisional obviousness-type double patenting rejection.

5. Claims 4, 5, 7-9 and 11-13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of copending Application No. 09/776,078 in view of Win et al.

Regarding claims 4 and 9 of the instant application, claim 7 of the '078 application discloses receiving a plurality of spatially diverse replicas of an RF signal, and adaptively combining the spatially diverse replicas to generate an equalized signal. Claim 7 of the '078 application does not expressly disclose that the combiner is part of an integrated circuit or a digital signal processor.

However, it is well known in the to implement portions of a digital receiver using integrated circuits and digital signal processors. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including integrated circuits and DSPs (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using an integrated circuit or a DSP as a matter of design choice as software and hardware implementations are well-recognized art equivalents.

Regarding claim 5 of the instant application, Win et al. disclose that the integrated circuit may be an ASIC.

Regarding claims 7 and 11 of the instant application, claim 3 of the '078 application discloses that an MLSE circuit is used.

Regarding claim 8 of the instant application, Win further discloses the combination of ASICs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a programmable ASIC configured by a microcontroller for implementing the combining means is deemed a design consideration that does not patentably distinguish over the prior art.

Regarding claim 12 of the instant application, Win further discloses the combination of DSPs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a general purpose DSP configured by a microcontroller for implementing the combining means is deemed a design consideration that does not patentably distinguish over the prior art.

Regarding claim 13 of the instant application, implementing tuners of the receiver and the DSP as an ASIC is deemed a design consideration that does not patentably distinguish over the prior art.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4-6, 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujimoto U.S. Patent 5,524,125 in view of Win et al. U.S. Patent 6,804,312.

Regarding claim 1, Tsujimoto discloses a receiver in Figure 2 for receiving a radio frequency signal comprising receiving a plurality of spatially diverse replicas of the RF signal (diversity reception signals 1 and 2) and adaptively combining the spatially diverse replicas to generate an equalized signal, S_d (see col. 7, lines 1-46), wherein the combining includes spatially equalizing each of the spatially diverse replicas in equalizers 101, 102, combining the spatially equalized replicas to form a combined signal via combiner 158, temporally equalizing the combined signal via decision feedback equalizer 105, and adapting the spatial and temporal equalizing steps to the symbol error signal via tap control circuits 103, 104, 106.

Tsujimoto does not expressly disclose that the receiver may be implemented in a computer readable storage medium containing a program.

However, it is well known in the art to implement a digital receiver using a program contained in computer readable storage medium. For instance, Win et al. disclose that a digital receiver for spatial processing that may be implemented with various software techniques (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the receiver of Tsujimoto using a software implementation where a computer program is stored in computer readable storage medium as a matter of design choice, as software and hardware implementations are well-recognized art equivalents.

Regarding claim 2, Tsujimoto further teaches generating a symbol error signal from the combined signal using symbol slicer circuit 109.

Regarding claim 4, Tsujimoto discloses an apparatus for receiving a radio frequency signal comprising a front end for receiving diverse replicas of the RF signal, selecting the RF signal from a frequency band, and digitizing the selected RF signal, as described in col. 6, lines 61-65, and means for combining the spatially diverse replicas of the RF signal to generate an equalized RF signal, where the means for combining includes feed forward equalizers 101, 102, a combiner 158 for combining the output signals from the feed forward equalizers to form a combined signal, an error circuit 109 for generating a symbol error signal, a decision feedback equalizer 105 for suppressing ISI, and tap control circuits 103, 104, 106 for adjusting tap weights of the feed forward equalizers and the decision feedback equalizer using the symbol error signal.

Tsujimoto does not expressly disclose that the combiner is part of an integrated circuit.

However, it is well known in the to implement portions of a digital receiver using integrated circuits. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including integrated circuits (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using an integrated circuit as a matter of design choice that fails to patentably distinguish over the prior art.

Regarding claim 5, Win et al. disclose that the integrated circuit may be an ASIC.

Regarding claim 6, Tsujimoto further teaches generating a symbol error signal from the combined signal using a slicer circuit including decision unit 107 and subtractor 109.

Regarding claim 8, Win further discloses the combination of ASICs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a

programmable ASIC configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish over the prior art of record.

Regarding claim 9, Tsujimoto discloses an apparatus for receiving a radio frequency signal comprising a front end for receiving diverse replicas of the RF signal, selecting the RF signal from a frequency band, and digitizing the selected RF signal, as described in col. 6, lines 61-65, and a combiner 158 for combining the spatially diverse replicas of the RF signal to generate an equalized RF signal, where the combiner includes feed forward equalizers 101, 102, a combiner 158 for combining the output signals from the feed forward equalizers to form a combined signal, an error circuit 109 for generating a symbol error signal, a decision feedback equalizer 105 for suppressing ISI, and tap control circuits 103, 104, 106 for adjusting tap weights of the feed forward equalizers and the decision feedback equalizer using the symbol error signal.

Tsujimoto does not expressly disclose that the combiner is part of a digital signal processor.

However, it is well known in the to implement portions of a digital receiver using DSPs. For instance, Win et al. disclose that digital receivers may be implemented with various circuit and software techniques, including DSPs (col. 11, lines 45-55).

It would have been obvious to one of ordinary skill in the art to implement the combiner of Tsujimoto using a DSP as a matter of design choice as software and hardware implementations are well-recognized art equivalents.

Regarding claim 10, Tsujimoto further teaches generating a symbol error signal from the combined signal using a slicer circuit including decision unit 107 and subtractor 109.

Regarding claim 12, Win further discloses the combination of DSPs and microcontrollers for performing various spatial processing operations (col. 11, lines 45-55). Use of a general purpose DSP configured by a microcontroller for implementing the combining means is deemed a design consideration that fails to patentably distinguish over the prior art of record.

Regarding claim 13, implementing the DSP as an ASIC is deemed a design consideration that fails to patentably distinguish over the prior art of record.

8. Claims 3, 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsujimoto in view of Win et al., and further in view of Liang et al. U.S. Patent 6,314,147.

Regarding claims 3, 7 and 11, Tsujimoto discloses a receiver as disclosed above, but does not expressly disclose that the error signal is generated using a maximum likelihood sequence estimation process.

Liang et al. disclose that the optimal solution to the problems of inter-symbol interference employs diversity combining and a maximum likelihood sequence estimator (col. 2, lines 50-56).

It would have been obvious to one of ordinary skill in the art to use a maximum likelihood sequence estimation process, as disclosed by Liang et al., in the diversity receiver of Tsujimoto for optimal correction of ISI.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Lugo
10/14/05

JAY K. PATEL
SUPERVISORY PATENT EXAMINER